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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,850	06/25/2003	Eugene A. Fitzgerald	MIT9888	5524
7	7590 09/23/2004		EXAMINER	
Attn: Matthew E. Connors			KESHAVAN, BELUR V	
Samuels, Gauthier & Stevens LLP Suite 3300			ART UNIT	PAPER NUMBER
225 Franklin Street			2825	
Boston, MA	02110		DATE MAILED: 09/23/2004	4

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	- ,			
Office Action Summan		10/603,850	FITZGERALD ET AL.				
	Office Action Summary	Examiner	Art Unit				
		Belur V Keshavan	2825				
Period fo	The MAILING DATE of this communication Reply	on appears on the cover sheet w	ith the correspondence address				
THE - Exte after - If the - If NC - Failt Any	ORTENED STATUTORY PERIOD FOR F MAILING DATE OF THIS COMMUNICAT nsions of time may be available under the provisions of 37 (SIX (6) MONTHS from the mailing date of this communicate period for reply specified above is less than thirty (30) days period for reply is specified above, the maximum statutory ure to reply within the set or extended period for reply will, by reply received by the Office later than three months after the ed patent term adjustment. See 37 CFR 1.704(b).	TION. CFR 1.136(a). In no event, however, may a ion. s, a reply within the statutory minimum of this period will apply and will expire SIX (6) MON y statute, cause the application to become Al	reply be timely filed ty (30) days will be considered timely. NTHS from the mailing date of this communicat BANDONED (35 U.S.C. § 133).	ion.			
Status							
1)⊠	Responsive to communication(s) filed on	25 June 2003.					
		This action is non-final.					
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposit	ion of Claims						
5)□ 6)□ 7)⊠	Claim(s) 1-21 is/are pending in the application of the above claim(s) is/are with Claim(s) is/are allowed. Claim(s) 1-21 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction	thdrawn from consideration.					
Applicat	ion Papers						
9)[The specification is objected to by the Exa	aminer.					
10)🛛	The drawing(s) filed on 25 June 2003 is/a	re: a)⊠ accepted or b)□ obje	ected to by the Examiner.				
	Applicant may not request that any objection	to the drawing(s) be held in abeya	nce. See 37 CFR 1.85(a).				
11)	Replacement drawing sheet(s) including the c The oath or declaration is objected to by t	·	• • •	• •			
Priority (under 35 U.S.C. § 119						
а)	Acknowledgment is made of a claim for for All b) Some * c) None of: 1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International Election for	uments have been received. uments have been received in A e priority documents have beer Bureau (PCT Rule 17.2(a)).	Application No I received in this National Stage				
Attachmen	t(s)						
1) Notic	e of References Cited (PTO-892)		Summary (PTO-413)				
2) Notice 3) Information	e of Draftsperson's Patent Drawing Review (PTO-94 mation Disclosure Statement(s) (PTO-1449 or PTO/5 r No(s)/Mail Date <u>3/27/2004</u> .	18) Paper No(s)/Mail Date nformal Patent Application (PTO-152)				

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DETAILED ACTION

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Fitzgerald et al. (PCT WO 02.15244 A2).

Regarding claims1, 7, 8, Fitzgerald et al. disclose, in claims and in specification, a method of bonding lattice-mismatched semiconductors comprising; forming a Ge based virtual substrate (claim 1 and lines 1-5); depositing a CMP layer of silicon oxide which is an oxide and comprises silicon on the virtual substrate that is polished to form a planarized virtual substrate (on page 4, lines 24-25 and 34-35 and claim 4); bonding a silicon substrate to the planarized virtual substrate (claim1 line 7 and page 4 lines 27-28); performing layer exfoliation on selective layers of the planarized virtual substrate producing a damaged layer of Ge and removing the damaged layer of Ge (claims 9,10 and 11 and page 5 lines 33-34 and page 6 lines 2-3).

Regarding claim 3, Fitzgerald et al. disclose that virtual substrate comprises a III-V transfer layer in claim 13 and on page 7 line 28.

Regarding claim 12, Fitzgerald et al. disclose, in claims and in specification a method of bonding lattice-mismatched semiconductors comprising; forming a virtual substrate (claim 1 and lines 1-5); using the virtual substrate to form a planarized virtual substrate substrate (on page 4, lines 24-25 and 34-35 and claim 4); bonding a silicon substrate to the planarized virtual substrate (claim1 line 7 and page 4 lines 27-28); and bonding a silicon substrate to the planarized virtual substrate (claim1 line 7 and page 4 lines 27-28) and removing selective layers of the planarized

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virtual substrate associated with the virtual substrate (claims 9,10 and 11 and page 5 lines 33-34 and page 6 lines 2-3).

Regarding claim 14, Fitzgerald et al. disclose that virtual substrate comprises a III-V transfer layer in claim 13 and on page 7 line 28.

Regarding claim 18, wherein the planarized virtual substrate is formed using oxide (on page 4, lines 24-25 and 34-35 and claim 4);

Regarding claim 19, wherein the planarized virtual substrate is formed using $Si_{1-x}Ge_x$ (in claim1 and age 7 and lines 4-5)

Regarding claims 2, 4, 5, 6, 9, 10,11, 13, 15, 16, 17, 20 and 21, the added "limitations" contained therein have not been given significant patentable weights as these method claims only provide statements of intended use of the layer or composition material of the layer and not any additional method step.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BVK. September 15, 2004.

Belur V. Keshavan. Examiner. Art Unit 2825. Page 4

MATTHEW SMITH SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800